UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,975,041 B2
APPLICATION NO. : 10/813038
DATED : December 13, 2005
INVENTOR(S) : Yuuichi Hirano et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 1 through Column 14, line 18, please replace the incorrect claims with the following:

Claims 1-3 (Canceled).

Claim 4. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 5. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

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said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 6. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and PMOS transistor having its gage electrode connected to said second power supply.

Claim 7. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

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Claim 8. The semiconductor storage device according to claim 7, which comprises a plurality of said first resistance-adding transistors.

Claim 9. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gage electrode connected to said first or second impurity-containing region.

Claim 10. The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

Claim 11. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and second access transistor which are connected to each other through a second storage noce, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

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said first resistance-adding transistor has its gate electrode connected to said work line.

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said work line.

Claim 12. The semiconductor storage device according to claim 4, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 13. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second stroage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gage electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetweeen,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.

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Claim 14. The semiconductor storage device according to claim 5, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 15. The semiconductor storage device according to claim 6, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 16. The semiconductor storage device according to claim 7, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 17. The semiconductor storage device according to claim 9, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 18. The semiconductor storage device according to claim 11, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

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Claim 19. The semiconductor storage device according to claim 13, further comprising:

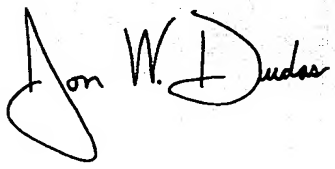
a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is conneted to said first storage node through said second resistance-adding transistor.

Signed and Sealed this

Fifth Day of September, 2006



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